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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/622,150	07/16/2003	Matthew Louis Courcy	NSC-P05579	1923

7590 09/29/2005

WAGNER, MURABITO & HAO LLP  
Third Floor  
Two North Market Street  
San Jose, CA 95113

EXAMINER

WILLIAMS, HOWARD L

ART UNIT PAPER NUMBER

2819

DATE MAILED: 09/29/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

## Office Action Summary

Application No.

10/622,150

Applicant(s)

COURCY, MATTHEW LOUIS

Examiner

Howard L. Williams

Art Unit

2819

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

### Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

### Status

- 1) ☒ Responsive to communication(s) filed on 12 September 2005.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

### Disposition of Claims

- 4) ☒ Claim(s) 1-3,5-9,11-15,17-21 and 23 is/are pending in the application.
- 4a) Of the above claim(s) \_\_\_\_\_ is/are withdrawn from consideration.
- 5) ☐ Claim(s) \_\_\_\_\_ is/are allowed.
- 6) ☒ Claim(s) 1-3,5-9,11-15,17-21 and 23 is/are rejected.
- 7) ☐ Claim(s) \_\_\_\_\_ is/are objected to.
- 8) ☐ Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

### Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on \_\_\_\_\_ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.  
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).  
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

### Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some \* c) ☐ None of:
- ☐ Certified copies of the priority documents have been received.
  - ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.
  - ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

\* See the attached detailed Office action for a list of the certified copies not received.

### Attachment(s)

- ☒ Notice of References Cited (PTO-892)
- ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)  
Paper No(s)/Mail Date \_\_\_\_\_.
- ☐ Interview Summary (PTO-413)  
Paper No(s)/Mail Date. \_\_\_\_\_.
- ☐ Notice of Informal Patent Application (PTO-152)
- ☐ Other: \_\_\_\_\_.

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 1-3, and 5 are rejected under 35 U.S.C. 102(b) as anticipated by U.S. P.A.P. 20020017936 A1 to Stark et al. Stark in figure 8 discloses: edge detectors (67a and 67b) and latch/S-R flip flop (66a).

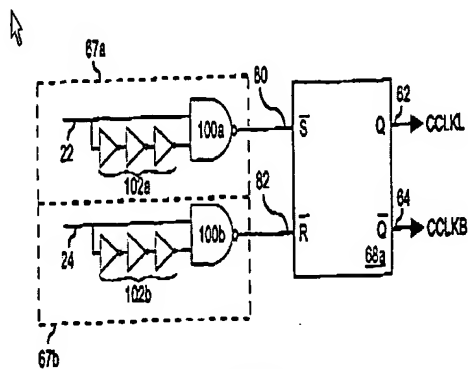
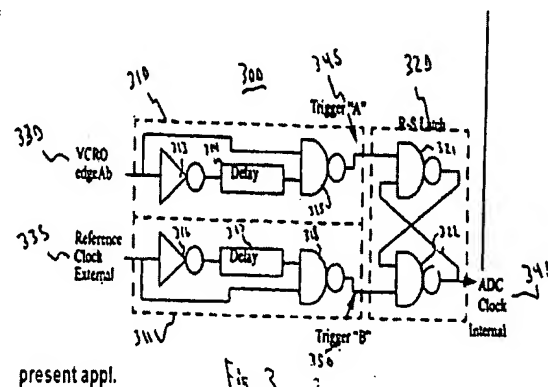


Figure 8



present appl.

Fig. 3

Stark's figure 8 (on the left above) has the same configuration as figure 3 of the present application since the inverters 102a and 102b provide delay circuits. The inputs (22, 24) to the Stark edge detectors are complementary clock signals and 180 degrees out of phase. In the terms of signal period and duty cycle would be one-half clock period delayed phase.

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

Claims 6-9, 11, 12 are rejected under 35 U.S.C. 103(a) as unpatentable over U.S. P.A.P. 20020017936 A1 to Stark et al. in view of Huynh (US 20030107432 A1).

Stark et al. does not mention ADC systems in particular but discloses two edge detectors side by side to the S input and R input, respectively, of an S-R flip-flop or latch, similar to applicants' embodiment. The clock duty cycle regulator of Stark et al. would have been an obvious choice to provide a 50% duty cycle clock signal because use of the a cleanly squared clock signal would provide a suitable clock to enable Huynh to achieve the desired well-timed output once each cycle thus increasing the circuit through-put and improving the applications such as data recovery.

Claims 13-15,17,18-21, and 23 are rejected under 35 U.S.C. 103(a) as unpatentable over U.S. P.A.P. 20020017936 A1 to Stark et al. in view of Huynh (US 20030107432 A1) and Davis (US 5394114 A). Stark discloses a clock generation circuit, duty cycle converter/corrector including two edge detectors supplying an S-R Flip-Flop serving as the claimed time generator or latch. Huynh supplies (from above) reasonable suggestion of well-timed clocks for an ADC. Stark does not elaborate on the clock generation circuit so does not disclose the claimed VCRO. Voltage controlled ring oscillators though are widely used to generate multiple-phased clock signals from an appropriately phased clock signal is selected. Davis discloses a voltage controlled ring oscillator to generate out of phase clock signals


The remarks filed 12 September 2005 have been fully considered but are not found persuasive.

The current response presents only minimal remarks addressing the Stark et al. reference. The statement on page 9 regarding the claims being amended to include separate signals could be seen as somewhat addressing Stark because the concluding sentence of paragraph says "references." Starks two inputs are seen to be separate signals in the same sense that the inputs in the claims are. Stark includes a clock signal (CLKL; 22; fig. 7) and inverted clock (CLKB, 24; fig. 7) these signals are disclosed as 180 degrees out of phase with each other and while they are generated from the same signal a conditioning circuit to produce the inverted CLKB, it is noted from the disclosure of the present application that the signal VCRO edgeAb is inverted

version of signal edgeA produced by the PLL. The application also discloses that many other "conditioning" circuits are suitable namely an inverter. In that the signal VCRO edgeAb is a delayed version of the external clock the claim and argument to the separateness is dubious at best. It is also noted that the latch circuit does not appear to receive an input from the conditioning circuit except through its interceding edge detector which the description refers to as "portion 310" thus the claims are questionable on two points 1) the reception of the second or conditioned signal by the latch from the conditioning circuit and 2) the edge detector being in fact two edge detectors.

Any inquiry concerning this communication should be directed to Howard L. Williams at telephone number 571.272.1815. The Patent and Trademark Office has a new central facsimile number for application specific correspondence intended for entry, it is 703-872-9306.

9/28/05  
Voice 571.272.1815

  
Howard L. Williams  
Primary Examiner  
Art Unit 2819